REMARKS/ARGUMENTS

Claims 1, 5, 9-12 and 16-21 remain pending in this application and stand rejected. In view of the foregoing amendment and following remarks, reconsideration of the rejections of these claims is respectfully requested.

Claim Rejections Under 35 USC § 112

Claims 1, 9-11, and 17-19 have been amended to overcome the rejections under 35 USC, 11, second paragraph.

Claim Rejections Under 35 USC § 103

Claims 1, 5, 11-12, 16-19, and 21 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Yamoto et al. US 7,089,517 (hereinafter Yamoto), in view of Liu et al. US 6,662,126 (hereinafter Liu), in view of Pramanick US 2004/0216005), and further in view of Beck et al. (US 6,624,829). Applicant respectfully traverses these rejections for at least the following reasons. Applicant submits that Yamoto fails to disclose any of the following steps of claim 1:

"generating a third waveform characterized as being a delayed replica of the first waveform and having transitions defining at least one launch edge;

generating a fourth waveform characterized as being a delayed replica of the second waveform and having transitions defining at least one latch edge;

selecting for display a portion of each of the first, second, third and fourth waveforms, the displayed portion of the third waveform comprising the at least one launch edge and the displayed portion of the fourth waveform comprising the at least one latch edge;

displaying pointers to time points of interest on the displayed waveform portions;

receiving edits to the time points of interest in response to a user moving the pointers on an interactive graphical user interface; and

modifying the circuit so as to cause a change in relative timing of the at least one launch edge and the at least one latch edge based on the edits to the time points of interest".

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The Examiner asserts that in column 7, lines 9-27, Yamoto discloses:

"display time points of interest on the displayed waveform portions....Thus, the edges of events (e.g., either a 0 to 1 transition or a 1 to 0 transition) are considered displayed time points of interest."

Applicant respectfully disagrees. The time points of interests refer to the simulation times, as shown for example in Figure 2, where the simulation times are shown inside the rectangles. Examiner's assertion that displaying "0 to 1" or "1 to 0" transitions are the same as displaying time points of interests is incorrect. Furthermore, claim 1 requires showing pointers to the time points of interest, which Yamoto fails to teach or suggest.

The Examiner asserts that in column 7, lines 24-27 Yamoto discloses:

"receive edits to the time points of interests n response to a user moving the time points of interest on the interactive graphical user interface. (7:24-27 "In the event bases test system, for example, an event may be inserted in a particular timing or an edge timing of an event may be changed through the event waveform editor/viewer 88"

Applicant submits that there is no disclosure in Yamoto of inserting an event in a particular timing or changing an edge timing of an event "in response to a user moving the pointers on an interactive graphical user interface", as required by claim 1. Yamoto's disclosure of using a waveform editor/view fails to satisfy this limitation. As best understood from the Office Action, the Examiner appears to acknowledge that Yamoto fails to teach or suggest "modifying the circuit so as to cause a change in relative timing of the at least one launch edge and the at least one latch edge based on the edits to the time points of interest", as required by claim 1.

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Claim 1 is thus allowable over Yamoto, whether taken alone or in combination with Liu, Pramanick and Beck.

The Examiner relies on Liu to supply a number of the limitations of claim 1 that the Examiner acknowledges are missing from Yamoto. In particular, Liu is cited by the Examiner as disclosing:

"receive the timing data from the on chip sampling, the timing data including at least multiple periods of a plurality of clock signals…" (3:11-17)

"enable selection of the first and second clock signal from the plurality of signals based on the an input received from a user…" (3:10-37)

"generate a first waveform for the first selected clock signal and a second waveform for the second selected clock signal using the timing data…" (Figure 5a, 4:61-65)

"generate a third waveform characterized as being a delayed replica of the first waveform and having transitions" (Figure 6 and 7:61-8:22)

"generate a fourth waveform characterized as being a delayed replica of the second waveform and having transitions" (Figure 6 and 7:61-8:22)

"select for display a portion of each of the first, second, third, and fourth waveforms" (Figure 6….)

Applicant respectfully traverses for at least the following reasons. Liu is directed at measuring skew of an on-chip signal on a computer chip. For example, the Abstract in Liu provides:

"A method and apparatus to determine skew of an on-chip signal without physical probing of the on-chip signal on the chip is provided. The method and apparatus use an externally generated reference signal that is distributed to one or more on-chip samplers that input the on-chip signal. Then, by modulating the externally generated reference signal,

transitions of the on-chip signal can be detected at the one or more on-chip samplers so that the skew of the on-chip signal can be determined."

Liu is completely silent on and has no relevance to using an EDA tool to simulate a circuit. Liu is a non-analogous art. Therefore, a person of ordinary skill in the art would not be motivated to combine the design validation technique of Yamoto with the skew measurement of an on-chip signal, as described by Liu. Claim 1 is thus further allowable over Yamoto, whether taken alone or in combination with Liu, Pramanick and Beck.

The Examiner relies on Pramanick to supply a number of the limitations of claim 1 that the Examiner acknowledges are missing from Yamoto and Liu. In particular, Pramanick is cited as disclosing:

"generate a waveform having transitions defining at least one launch edge (Figure 4B and 5A-5C and paragraphs 0043-0046 describe two flip-flops and their associated timing diagrams....signal b at arrow 62 is considered the launch edge of the first clock signal....."

"generate a waveform having transitions defining at least one latch edge ((Figure 4B and 5A-5C and paragraphs 0043-0046 describe two flip-flops and their associated timing diagrams....signal d at arrow 64 is considered the latch edge of the edge of the second clock signal....."

"select for display a portion of each of the waveforms, the displayed portion of a first waveform comprising the at least one launch edge and the displayed portion of a second waveform comprising the at least one latch edge (Figures 4B, and 5A-5C and paragraphs 0043-0046..."

"modify the circuit so as to cause a change in relative timing of the at least one launch edge and the at least one latch edge based on edits to the time points of interest (0043-0047 and Figures 5A-5C....)

Applicant respectfully traverses for at least the following reasons.

Both signals "b" and "d" shown in Figures 4B and 5A of Pramanick are generated in response to clock signal "CLK" applied to the clock input terminals of flip-flops 51 and 53. Block 52 is a random logic that generates signal "c" in response to signal "b", as disclosed in paragraph 43 of Pramanick:

"In FIG. 4B, "CLK", "a", "b", "c" and "d" respectively represent a clock signal for the flip-flops 51 and 53, an input of the flip-flop 51, an input of the random logic 52, an input of the flip-flop 53, and an output of the flip-flop 53. The clock "CLK", input "a" and output "d" in FIG. 4B respectively correspond to the clock "CLK", input "a" and output "d" in FIG. 4A."

Applicant points out that claim 1 requires that the "first and second clock signals" be selected "from the plurality of clock signals". Furthermore, claim 1 requires that the third waveform be characterized as "a delayed replica of the first waveform", and that the fourth waveform be characterized as "a delayed replica of the second waveform". Signals "b" and "d" are not clock signals and fail to satisfy the required limitations of claim 1.

Referring to paragraphs 0043-0047 and Figures 5A-5C, the Examiner refers to the following excerpts from Pramanick:

"[0045] In FIG. 5B, suppose that due to a certain reason, the propagation delay .DELTA.bc2 through the random logic 52 is significantly larger than the normal propagation delay .DELTA.bc1 of FIG. 5A. Due to this large delay, the value at the input "c" of the flip-flop 53 remains "0" at the edge of clock (clk3). Hence, the output "d" of the flip-flop 53 is also in the "0" state at the timing of the strobe 65, which shows an incorrect value...."

"The cause of this failure is the excessive delay through the random logic 52 for the signal to propagate from the input "b" to the output "c"...."

"In FIG. 5C, if an extra time 66a and 66b is added between the clock clk2 and clock clk3 (also to the strobe 65), the value at the input "c" of the flip-flop 53 changes to "1" before the rising edge of the clock clk3. As a result, the value at the output "d" of the flip-flop 53 changes to "1" with the rising edge of the clock clk3, which shows the correct value.."

to make the following assertion:

" Thus the circuit has been modified so as to cause a change in relative timing of the at least one launch edge and the at least one latch edge based on the edits to the time points of interest".

Applicant respectfully disagrees. In the above excerpts, Pramanick appears to state that by adding the additional time of 66a and 66 between clk2 and clk3, the correct value is obtained at the output of flip-flop 52. To achieve this, Pramanick appears to increase the width of the second pulse (clk2) of signal CLK which, in turn, affects the timing delay between signals b and d. However, as noted above, signals b and d are not clock signals.

Claim 1 is thus allowable over Yamoto, whether taken alone or in combination with Liu, Pramanick and Beck. Claims 5 and 9-10 are dependent from claim 1 and are thus allowable for at least the same reasons as is claim 1. Claim 11 and its dependent claims 12, 16-21 are allowable for at least the same reasons as is claim 1.

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

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